

AMENDMENTS TO THE CLAIMS

Please cancel claims 31-49 without prejudice or disclaimer of their underlying subject matter.

1. (original) A nonvolatile semiconductor memory device comprising:

a substrate;

a semiconductor channel forming region in the vicinity of the surface of the substrate;

a first and a second impurity regions formed in the vicinity of the surface of the substrate sandwiching the channel forming region between them, acting as a source and a drain in operation;

a gate insulating film stacked on the channel forming region, and comprised of a plurality of films;

a gate electrode formed on the gate insulating film;

a charge storing means which is formed in the gate insulating film dispersed in the plane facing the channel forming region and in the direction of thickness and is injected with excited hot electrons in operation due to an electric field applied; and

wherein a bottom insulating film positioned at the bottom in said gate insulating film comprises

a dielectric film that makes an energy barrier between the bottom insulating film and the substrate lower than that between silicon dioxide and silicon.

2. (original) A nonvolatile semiconductor memory device as set forth in claim 1, wherein said bottom insulating film comprises a dielectric film that makes an energy barrier between the bottom insulating film and the substrate lower than that between silicon and an oxynitride film formed after silicon dioxide is nitrided.

3. (original) A nonvolatile semiconductor memory device as set forth in claim 2, wherein the percentage of nitrogen content in said oxynitride film is not greater than 10%.

4. (original) A nonvolatile semiconductor memory device as set forth in claim 1, wherein in a write or erasure state, said charge storing means is primarily injected with anyone of channel hot electrons, ballistic hot electrons, secondarily generated hot electrons, substrate hot electrons, and hot electrons caused by band-to-band tunneling current.

5. (original) A nonvolatile semiconductor memory device as set forth in claim 1, wherein said dielectric film included in said bottom insulating film exhibits a Fowler-Nordheim (FN) type tunneling electroconductivity.

6. (original) A nonvolatile semiconductor memory device as set forth in claim 1, wherein said bottom insulating film includes said dielectric film comprised of anyone or a combination of a silicon nitride film, a silicon oxynitride film, a tantalum oxide film, a zirconium oxide film, an aluminum oxide film, a titanium oxide film, a hafnium oxide, a barium strontium titanium oxide, and an yttrium oxide film.

7. (original) A nonvolatile semiconductor memory device as set forth in claim 1, wherein, said gate insulating film comprises a nitride film or an oxynitride film exhibiting a Frenkel-Pool (FP) type electroconductivity on said bottom insulating film.

8. (original) A nonvolatile semiconductor memory device as set forth in claim 1, wherein said gate insulating film comprises:

a first region into which the hot electrons are injected from said first impurity region;

a second region into which the hot electrons are injected from said second impurity region; and

a third region between the first and the second impurity regions into which the hot electrons are not injected.

9. (original) A nonvolatile semiconductor memory device as set forth in claim 1, wherein said gate insulating film comprises:

a first region at the side of said first impurity region;

a second region at the side of said second impurity region; and

a third region between the first and the second regions,

wherein said charge storage means is formed in the first and the second regions; and

wherein the distribution region of the charge storing means is spatially separated by the third region.

10. (original) A nonvolatile semiconductor memory device as set forth in claim 9, wherein

said first and second regions are stacked film structures comprised of a number of films stacked together, and

said third region is a single layer of a dielectric.

11. (original) A nonvolatile semiconductor memory device as set forth in claim 9, wherein a gate electrode formed on said third region is spatially separated from gate electrodes formed on said first region and second regions.

12. (original) A nonvolatile semiconductor memory device as set forth in claim 1, comprising:

a plurality of memory transistors each of which including said channel forming region, said first and second impurity regions, said gate insulating film, and said gate electrodes, and arranged in both a word line direction and a bit line direction;

a plurality of word lines; and

a plurality of common lines which intersect with the plurality of word lines in an electrically insulated state,

wherein the plurality of gate electrodes are respectively connected to the plurality of word lines; and

wherein the plurality of the first and second impurity regions are coupled with the plurality of common lines.

13. (original) A nonvolatile semiconductor memory device as set forth in claim 12, comprising:

word lines commonly connecting said gate electrodes in a word line direction;

first common lines commonly connecting said first impurity regions in a bit line direction; and

second common lines commonly connecting said second impurity regions.

14. (original) A nonvolatile semiconductor memory device as set forth in claim 13, wherein:

said first common lines include first sub-lines commonly connecting said first impurity regions in a bit line direction and first main lines commonly connecting the first sub-lines in a bit line direction;

said second common lines include second sub-lines commonly connecting said second impurity regions and second main lines commonly connecting the second sub-lines; and

said plurality of memory transistors are connected in parallel between the first sub-lines and the second sub-lines.

15. (original) A nonvolatile semiconductor memory device as set forth in claim 1, wherein

said charge storing means does not have conductivity as a plane as a whole facing said channel forming region at least when there is not dissipation of charge in the outside.

16. (original) A nonvolatile semiconductor memory device as set forth in claim 15, wherein said gate insulating film comprises:

a bottom insulating film on said channel forming region;

a nitride film or an oxynitride film on said bottom insulating film; and

a top insulating film on said nitride film or oxynitride film.

17. (original) A nonvolatile semiconductor memory device as set forth in claim 15, wherein said gate insulating film comprises:

a bottom insulating film on said channel forming region, and

a top insulating film on said bottom insulating film.

18. (original) A nonvolatile semiconductor memory device as set forth in claim 17, wherein the Si-H bond density in the bottom insulating film is lower than that in the nitride film that shows a FP type electroconductivity and constitutes said top insulating film.

19. (original) A nonvolatile semiconductor memory device as set forth in claim 18, wherein the Si-H bond density in the bottom insulating film is lower than 1×10^{20} atoms/mm³.

20. (original) A nonvolatile semiconductor memory device as set forth in claim 19, wherein the Si-H bond density in the bottom insulating film is by more than one order of magnitudes lower than that in the nitride film showing a FP type electroconductivity and constituting said top insulating film.

21. (original) A nonvolatile semiconductor memory device as set forth in claim 17, wherein said bottom insulating film comprises a buffer oxide film on said channel forming region and a dielectric film that is formed on said buffer oxide film and is comprised of a material having a dielectric constant greater than that of silicon dioxide.

22. (original) A nonvolatile semiconductor memory device as set forth in claim 17, wherein said bottom insulating film comprises:

a dielectric film formed on said channel forming region and comprised of a material having a dielectric constant greater than that of silicon dioxide and

a silicon dioxide film formed on the dielectric film.

23. (original) A nonvolatile semiconductor memory device as set forth in claim 15, wherein said gate insulating film comprises:

a bottom insulating film on said channel forming region and

mutually insulated small particle conductors formed on the bottom film and functioning as said charge storing means.

24. (original) A nonvolatile semiconductor memory device as set forth in claim 23, wherein said small particle conductors are of diameters not greater than 10 nanometers.

25. (original) A nonvolatile semiconductor memory device comprising:

a substrate;

a semiconductor channel forming region in the vicinity of the surface of the substrate;

a first and a second impurity regions formed in the vicinity of the surface of the substrate sandwiching the channel forming region between them, acting as a source and a drain in operation;

a gate insulating film stacked on the channel forming region and comprised of a plurality of films;

a gate electrode formed on the gate insulating film; and

a charge storing means which is formed in said gate insulating film dispersed in the plane facing said channel forming region and in the direction of thickness and is primarily injected in operation with channel hot electrons, ballistic hot electrons, secondarily generated hot electrons, substrate hot electrons, and hot electrons caused by band-to-band tunneling current, and

wherein a bottom insulating film positioned at the bottom in the gate insulating film comprises a dielectric film of a material having a dielectric constant greater than that of silicon dioxide.

26. (original) A nonvolatile semiconductor memory device as set forth in claim 25, wherein the Si-H bond density in said bottom insulating film is lower than that in a nitride film showing a FP type electroconductivity and constituting said gate insulating film.

27. (original) A nonvolatile semiconductor memory device as set forth in claim 26, wherein the Si-H bond density in said bottom insulating film is lower than 1×10^{20} atoms/mm³.

28. (original) A nonvolatile semiconductor memory device as set forth in claim 27, wherein the Si-H bond density in said bottom insulating film is by more than one order of magnitudes lower than that in a nitride film showing a FP type electroconductivity and constituting said gate insulating film.

29. (original) A nonvolatile semiconductor memory device comprising:

a substrate;

a semiconductor channel forming region in the vicinity of the surface of the substrate;

a first and a second impurity regions formed in the vicinity of the surface of the substrate sandwiching the channel forming region between them, acting as a source and a drain in operation;

a gate insulating film stacked on the channel forming region and comprised of a plurality of films;

a gate electrode formed on the gate insulating film; and

a charge storing means which is formed in said gate insulating film dispersed in the plane facing said channel forming region and in the direction of thickness and is primarily injected in operation with channel hot electrons, ballistic hot electrons, secondarily generated hot electrons, substrate hot electrons, and hot electrons caused by band-to-band tunneling current,

wherein the gate insulating film comprises:

a first region at the side of the first impurity region;

a second region at the side of the second impurity region; and

a third region between the first and the second regions,

wherein said charge storage means is formed in the first and the second regions; and

wherein the distribution region of the charge storing means is spatially separated by the third region.

30. (original) A nonvolatile semiconductor memory device as set forth in claim 29, wherein

said first and second regions are stacked film structures comprised of a number of films stacked together, and

said third region is a single layer of a dielectric.

31-49. (canceled)